REMARKS

Claims 1-14 and 29, 31-38, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 5-6, 8, 12-13, 29, 32, 34-35, and 37-38 stand rejected under 35 U.S.C. §102(e) as being anticipated by She, et al. (U.S. Publication No. 2005/0242391), hereinafter referred to as She. Claims 1, 3-4, 7-8, 10-11, 14, 29, and 34 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Hsu, et al. (U.S. Patent No. 6,107,141), hereinafter referred to as Hsu. Claims 2, 9, 31, and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over She. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a multiple-gate transistor comprising a logic gate, a floating gate, and a programming gate, which the Office Action argues is disclosed in She. However, the structure of She only has two gates, wherein the alleged "trapping layer" of She does not affect the channel region and therefore does not disclose a gate structure. Further, the gate 1 and the gate 2 of She each perform the same function, i.e., they are both "control gates"; thus, a logic gate is not disclosed. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action argues that She discloses a floating gate (Office Action, pp. 3-4, item no. 3). More specifically, referencing figures 10 and 11 of She, the Office Action argues that a trapping layer (where Bit 1 and Bit 2 are trapped) is analogous to the floating gate of the claimed invention.

Applicants respectfully disagree with such a conclusion. Specifically, the alleged trapping layer of She is not a gate.

First of all, even if the Office Action is correct that the silicon nitride (see FIGS. 1, 2E, and 2G) might hold charges does not mean that it is any form of gate. Just because a layer holds charge does not necessarily make it a gate. As is commonly known within the art, a gate activates or changes the characteristic of a channel region by turning the channel region on or off, adjusting the threshold voltage of the channel region, etc. So unless the structure in She has some affect on the channel region, it would not teach a gate structure. It appears from the vague description of She that the nitride regions act merely as storage capacitors. They do not have any affect on the channel; and therefore, the regions cannot be gates.

Moreover, Applicants submit that even if the Office Action is correct that the "Bit 1" and the "Bit 2" structures store charge, the silicon nitride component between the Bit 1 and the Bit 2 does not store charge. There are 3 separate components in the area that the Office Action asserts teaches the floating gate (see FIGS. 1, 2E, and 2G).

Furthermore, figures 10 and 11 and the accompanying text only disclose two (2) gates: gate 1 (which the Office Action asserts teaches the logic gate of the claimed invention); and, gate 2 (which the Office Action asserts teaches the programming gate of

the claimed invention). More specifically, paragraph 0035 of She provides that "[t]here are source storage bit and drain storage bit (*two bits/gate*) associated with each gate, hence a *total* of 4 physical bit/cell is realized with the above structure."

Since there are only four 4 "total" bits shown, and two bits are provided per gate, only two gates are disclosed figures 10 and 11 (i.e., gate 1 and gate 2). If the trapping layer were a gate, there would be three total gates and six total bits shown. However, figures 10 and 11 and the accompanying text clearly show that the structure only has four total bits (See paragraph 0035 of She, "hence a total of 4 physical bit/cell is realized with the above structure").

Accordingly, Applicants submit that She fails to teach a logic gate, a programming gate, and a floating gate. Instead, She discloses a structure having only two gates. The alleged "trapping layer" of She does not affect the channel region and therefore does not disclose a gate structure. As such, it is Applicants' position that She fails to the claimed feature of "A multiple-gate transistor comprising ... a floating gate" as defined by independent claims 1, 8, 29, and 35.

The Office Action also argues that She discloses a floating gate that adjusts the threshold voltage of the transistors because "this is inherent characteristics of floating gate transistor" (Office Action, p. 8, para. 1). Such features are defined in independent claims 29 and 34, and in dependent claims 4 and 11, using similar language.

As discussed more fully above, the alleged trapping layer of She does not teach a floating gate. Therefore, contrary to the position taken in the Office Action, She does not inherently teach a floating gate that adjusts the threshold voltage of the transistors.

In addition, the Office Action argues that She discloses a logic gate (Office Action, p. 3, item 3, citing figures 10-11 of She). Applicants respectfully disagree with such a conclusion. Instead, She discloses a structure having two control gates and zero logic gates.

Specifically, as provided in paragraph 0032 of She, a 4 physical bit/cell can be realized by breaking the top portion of the control gate on top of each channel. For example, a folded control gate in FIG. 6A is broken into *two control gates* by using a chemical mechanical polishing (CMP) method. As shown in FIG. 8, these *two control gates* control each vertical side of the channel region. Here the front gate is called "gate1" and the back gate is called "gate 2" in each memory cell.

The Office Action asserts that the gate 1 of She is a logic gate (Office Action, p. 3, item 3). However, as discussed above, the gate 1 is a control gate, not a logic gate. Therefore, Applicants submit that, contrary to the position taken in the Office Action, She fails to teach the claimed feature of a logic gate, as defined by independent claims 1, 8, 29, and 35, "wherein voltage in said logic gate causes said transistor to switch on and off" as defined by independent claims 29 and 35.

Moreover, even if the Office Action is correct in that the gate 1 is a logic gate and that the gate 2 is a programming gate, the gate 1 and the gate 2 each perform the same function, i.e., they are both "control gates" (She, para. 0032). Therefore, She fails to teach the claimed feature "wherein said logic gate performs a different function than said floating gate, wherein said logic gate performs a different function than said programming gate, and wherein said floating gate performs a different function than said

programming gate" as defined by independent claims 1 and 8. Additionally, She fails to teach the claimed feature "wherein voltage in said logic gate causes said transistor to switch on and off ... and wherein charge in said floating gate adjusts the threshold voltage of said transistor" as defined by independent claims 29 and 35.

Furthermore, Applicants traverse the rejections because Hsu fails to disclose that that the first side of the channel region is opposite the second side of the channel region such that the channel region is between the first side and the second side. Such features are defined in independent claims 1, 8, 29, and 35 using similar language.

The Office Action argues that Hsu discloses a channel region having a first side which is directly under the gate 120 and a second side which is right under the gate 130 (Office Action, p. 4, para. 2). However, Hsu does not teach a channel region *between* the alleged "first side" and the alleged "second side". Instead, the channel region is *below* the alleged "first side" and the alleged "second side"

More specifically, the portion of the substrate 10 that is between the source 30 and the drain 20 is the channel region of Hsu. This channel region is not between the side of the channel region that is below the gate 120 (which the Office Action asserts is analogous to the first side of the claimed invention) and the side of the channel that is below the gate 130 (which the Office Action asserts is analogous to the second side of the claimed invention). Instead, the channel region is below the alleged "first side" and the alleged "second side".

Accordingly, it is Applicants' position that Hsu fails to teach the claimed feature of "a logic gate adjacent a first side of said channel region ... [and] a floating gate

adjacent a second side of said channel region, wherein said first side is opposite said second side such that said channel region is between said first side and said second side" as defined by independent claims 1, 29, and 35. Further, Hsu fails to teach the claimed feature of "a gate oxide on a first side of said channel region ... [and] a first insulator on a second side of said channel region, wherein said second side of said channel region is opposite said first side such that said channel region is between said first side and said second side" as defined by independent claim 8.

Therefore, it is Applicants' position that neither She nor Hsu disclose many features defined by independent claims 1, 8, 29, and 35 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-14, 31-34, and 36-38 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-14, 29, 31-38, all the claims presently pending in the application, are patentably distinct from the prior art of

record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 10/18/06

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